Noise free and jitter-less clock distribution method for high-frequency system using microcavity

H. Kato, E. Kondoh, T. Akitsu, T. Kobori and H. Morishita
University of Yamanashi, Interdisciplinary Graduate School of Medicine and Engineering
4-3-11 Takeda, Kofu, Yamanashi 400-8511, Japan

ABSTRACT

The clock frequency in ULSI systems increases year by year and will exceed 10GHz. At these frequencies the signal propagation in a conventional bus line is affected by high-frequency effects causing propagation delay and noise emission. Here, we propose a novel method of using a cavity for clock delivery. Because the clock signal is enclosed in metallic walls, this system does not generate high frequency noise. Moreover, the jitter-less clock can be delivered everywhere in ULSI chip, if a high *Q*-factor is realized.

When the clock frequency in a ULSI system reaches 10GHz, a conventional global bus line is involved in the noise generation and the increase of propagation delay because of the skin effect [1-2]. Recently, several proposals have been made to solve these problems such as by using a multi-buffered driver [1], a combination of an optical and electric system [3] and a wireless distributor [4-5]. Although these methods have their own advantages, there have been few considerations about the noise generation from the global bus lines. As the scaling down of transistors proceeds, a much lower voltage supply is required because of device reliability and the ULSI system will be much more affected by high-frequency noise due to global bus lines. In our novel method a cavity encloses the clock signal inside metallic walls and completely separates the clock signal from circuit elements on the ULSI chip, so that there is no need to worry about noise generation.

The chip size of the ULSI is more than 10mm and the length of the global line is also reaching tens of millimeters. Therefore, there are remarkable discrepancies between propagation delays due to the variation of wire length. The H-tree or dog-bone configuration is a method to solve this problem, where the global lines have high geometrical symmetry for all propagation paths [6]. When the clock frequency increases, the reflections in the bus line will be pronounced and its design will be difficult. On the other hand, a resonance mode in our cavity is spatially uniform and its frequency is determined uniquely by dimensions of the cavity, so that we can deliver spatially uniform and stable clock to everywhere on chip.

When the clock frequency reaches 10GHz, its wavelength becomes a few millimeters and is less than the size of ULSI chip, therefore, the aforementioned cavity will be realizable on a chip. At the frequency f the skin depth δ is given by $\delta = (\pi f \sigma \mu)^{-1/2}$, where σ is the conductivity of bus line and μ is the magnetic permeability. When the cavity wall is made of Cu, a usual material of metallization, and the frequency is over than 10GHz, the skin depth δ is less than 1μm, a typical

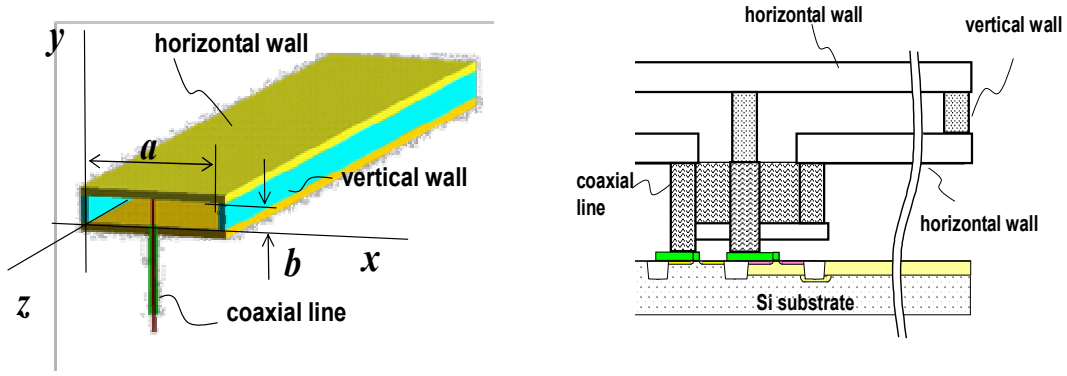
metal thickness. Therefore, as the frequency increases, the microwave is enclosed gradually in a cavity and the high frequency noise is suppressed.

A possible cross section of the cavity is illustrated in Figure 1 (a), where the vertical scale is magnified for convenience sake. The width a of the cavity must be greater than the half of the wavelength. The horizontal walls of the cavity are fabricated by a usual metallization process of Cu. The side walls can also be fabricated by a usual via process. Although the side wall in the figure is continuous, an array of via pillars fulfills the requirement, because the wave length is a few millimeters and much greater than 1μm a typical diameter of via contact. If the cavity size is $a \times b \times c$ and a cavity mode is TE_{10} with n the mode index in z-direction, the resonance frequency f is given by

$$f = \frac{1}{2}\sqrt{\frac{1}{\varepsilon\mu}\left(\frac{1}{a^2}+\frac{n^2}{c^2}\right)}, \tag{1}$$

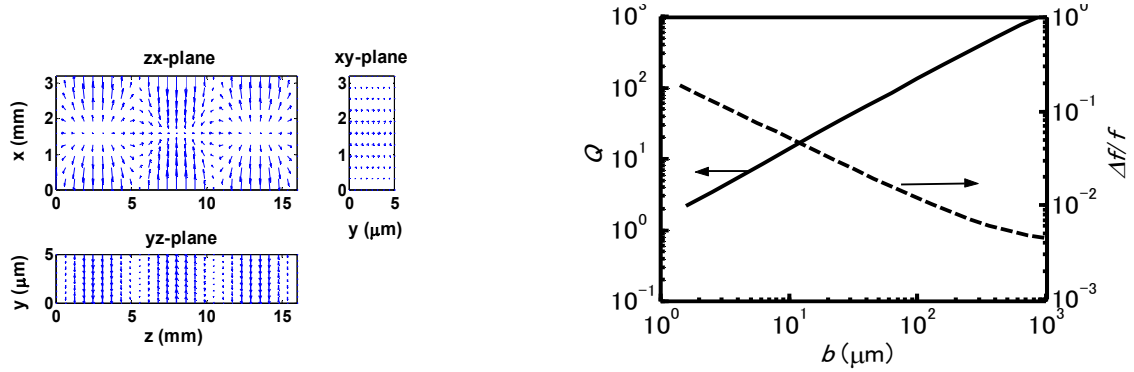
where ε and μ are the dielectric constant and magnetic permeabilityof a filler (SiO_2) respectively. It is possible to realize a desired frequency by adjusting the cavity dimensions and mode index n. When we use a = 3.2mm, b = 5μm, c = 16mm and n = 3, the resonance frequency becomes 27GHz and the skin depth of Cu wall is 0.40μm. This skin depth is almost half of a typical metal thickness and there is little possibility that the fields leak to the outside of the cavity.

If the transistor power performance is high enough, an on-chip driver is possible and desirable to excite the cavity. However an external driver located outside of the ULSI chip is more realizable. A coaxial line shown in the Figure 1 is an example to guide the resonant signal outside. The guide line to pick up the cavity signal must be located at the point where the electric field reaches maximum. This coaxial line is also possible to be fabricated by a usual via process and does not require any new process.



(a) (b)

Figure 1. A schematic diagram of a cavity (vertical axis not to scale) (a). The clock is delivered by a coaxial line made by a via process (b). The top and lower horizontal walls can be realized by metallization process, the vertical wall and the coaxial line will be formed by a via process.



(a) (b)

Figure 2. The vector plot of current density at cavity walls (a). The thickness b dependence of the Q -factor and the half width of the resonance curve Δf normalized by the resonance frequency f (b). The cavity mode is TE_{10} with the index n = 3 and the wall material is Cu lined with Ta barrier metal of 20nm thickness.

The electric current density on cavity walls is determined by the mode of electromagnetic wave. A vector plot of electric currents for TE_{10} mode with the mode index n = 3 is shown in Figure 2 (a). When the cavity is fabricated by a former process of alumnum wire and tungsten via, the density of the energy loss reaches its maximum at the side wall (yz-plane) because its material has large resistance compared with the horizontal material. However, the dominant loss occurs at the horizontal walls and its amount remains relatively small. Even if the side walls are fabricated by an array of via pillars, the current flow and resonance mode in the cavity do not be disturbed because the direction of currents at the side wall is vertical.

The jitter of the clock is subjected by the resonance curve of the cavity and it is characterized by Q-factor. The Q-factor is defined by $Q = Uf/P$ with U the electromagnetic energy in the cavity, f the resonance frequency given by equation (1) and P the energy loss per unit time due to currents on the walls:

$$Q = \frac{4f\mu abc(c^2 + a^2n^2)}{(R_{HU} + R_{HL})(c^2 + na^2)ca + 2R_V(c^3 + na^3)b} \quad . \tag{2}$$

Here, n is the mode index in z-direction, R_{HU}, R_{HL} and R_V are sheet resistances of horizontal-upper , horizonal-lower and vertical walls respectively. If the metallic walls are made by Cu metallization lined with Ta barrier metal of depth d and conductance σ_B, the sheet resistance of horizontal lower wall is $R_{HL} = 1/\delta_L\sigma_{LHL}$ and the resistances of horizontal upper and side wall are given by

$$R_p = \frac{\cosh(d/\delta_B) + \sqrt{\sigma_p/\sigma_B}\ \sinh(d/\delta_B)}{\{\sinh(d/\delta_B) + \sqrt{\sigma_p/\sigma_B}\ \cosh(d/\delta_B)\}\sigma_B\delta_B + \sigma_p\delta_p} \quad (p = HU, V), \tag{3}$$

where σ_p is conductance and $\delta_p = (\pi f\mu\sigma_p)^{-1/2}$ is the skin depth of horizontal (p=HU) and vertical (p=V) materials. In Figure 2(b) the thickness b dependence of the Q-factor is shown. The barrier

metal is assumed to be Ta, which has a large resistance compared with the wall material Cu but its thickness is 20nm and less than the skin depth. Therefore, the effect of a barrier metal on *Q*-factor is week. With an increase in *b* the value of *Q* increases monotonically because the energy *U* increases with *b*. The saturation of curve about *Q* is caused by the fact that the energy loss due to the side wall increases with *b* and becomes comparable to that of the horizontal walls.

Although, the frequency distribution of resonance mode depends on the feature of cavity driver, an upper bound of the clock jitter is estimated by the half width of the resonant curve. Using a model of damped oscillator, the half width Δf is expressed by

$$\frac{\Delta f}{f} = \left(\frac{16\pi^2 Q^2 - 1}{4\pi^4 Q^4} \right)^{1/4} . \tag{4}$$

In Figure 2 (b) the half width given by equation (2) is also plotted by dashed line and its value is about several tens of percents. This implies that not only high *Q* but also the frequency control on cavity driver is also important to suppress the clock jitter. At least the value of *Q*-factor must be greater than two and the cavity thickness must be more than 5μm, but a desirable *Q*-value is several tens and the thickness *b* must be more than 10μm. A typical process is hard to form a insulator layer (SiO_2) more than 1μm. However, with combination of stuck via and metallization process can achieve the thickness *b* of 5μm. On the other hand, a fabrication technique of 10~100μm scale components has been discussed recently to achieve a high performance assembly [1] and a technical development to form a thick Cu layer is already realized [7]. This technology can be used to form our cavity so as to obtain high *Q*.

In this paper we discussed a possibility of using a micro cavity to deliver high clock signal over than 10GHz. A typical size of the cavity is 3.2mm×5μm×16mm and its resonance frequency is 27GHz. The cavity is realizable because it can be formed by a usual metallization and via process.

REFERENCES

1. T. Sakurai, in proceedings of *Advanced Metallization Conference 2000* edited by D. Edelstein, G. Dixit, Y. Yasuda and T. Ohba, (Mater. Res. Soc, Warrendale PA, 2000) pp.53-58.
2. N. Takagi, H. Shinoki, K. Masu, in proceedings of *Advanced Metallization Conference 2001* edited by A.J. McKerrow, Y. Shacham-Diamand, S. Zaima and T. Ohba, (Mater. Res. Soc, Warrendale PA, 2001) pp.121-125.
3. P. Kapur and K. C. Saraswat, Physica E **16**, 620 (2003).
4. K.Kim, W. Bomstad and K. K. O, in digest of *International Symposium 2001 of IEEE Anntena & Propagation Society*, vo.2, (IEEE, Piscataway, NJ, 2001)pp.166-169.
5. A.B.M.H. Rashid, S. Watanabe, T. Kikkawa, T, IEEE Electron Device Lett. **23,** 173 (2002).
6. M. Mizuno, K. Anjo, Y. Surni, H. Wakabayashi, T. Mogami, T. Horiuchi and M. Yamashina, in proceedings of *International Solid-State Circuits Conference 2000*, (IEEE, Piscataway NJ, 2000) pp.366-367.
7. K. Kikuchi, M. Takamiya, Y. Kudoh, K. Soejima, H. Honda, M. Mizuno and S. Yamamichi, in proceedings of International Interconnect Technology Conference 2003, (IEEE, New York 2003) pp.189-191.