SRAM Cell Stability Under the Influence of Parasitic Resistances and Data Holding Voltage as a Stability Prober

H. Kato, M. Matsui, K. Sato, H. Shibata, K. Hashimoto, T. Ootani, and K. Ochii

Abstract—**The reliability and performance of SRAM are highly dependent on the cell stability, and the stability is affected by parasitic resistances in a memory array. The parasitic resistances result in a correlative behavior of the cells and are difficult to analyze and measure in a memory array. This topic has been rarely discussed in the literature. In this paper, the correlative behavior is analyzed by trajectories in a phase diagram composed by cell storage nodes. Electrical probing is done by the data holding test. The validity of the analysis and the probing method is confirmed by the measurements on a 0.8-μm 1-Mb CMOS SRAM. An aspect on the cell scaling with attention to the parasitic resistance is also discussed.**

Index Terms— **Approving Test, cell stabilit, parasitic resistancey, scaling, SRAM, VLSI.**

I. Introduction

THE reliability and the performance of SRAM is highly dependent on the cell stability, and it is increasingly difficult to maintain and improve the stability while migrating to high density and small geometry devices. A number of factors which degrade the stability are known, e.g., leakage paths, defectivity, and alpha hit rate [1]–[3]. In this paper, we pay attention to the parasitic resistances of the wires in memory array. The resistances result in a correlative behavior between the cells. As the fabrication migrates to smaller geometries, the parasitic resistances are enhanced by wiring width reduction, low temperature process to restrict the lateral impurity diffusion, and layer misalignment such as contact holes [1].

A regular method to evaluate the cell stability is the static noise margin (SNM) analysis. There are several reports on theory [4]–[6] and measurement [1] of the SNM for an isolated cell. However, they do not deal with the effect of parasitic resistances because the effect appears in the memory array. We employ the data holding test to discuss the cell correlation caused by the parasitic resistances in an actual environment. The transient cell behavior in the test sequence is explained by a trajectory in the phase plane formed by two storage nodes of a cell. The trajectory analysis is already employed to discuss the alpha-particle immunity [7], [8], however, this is the first attempt to apply the analysis on the data holding test.

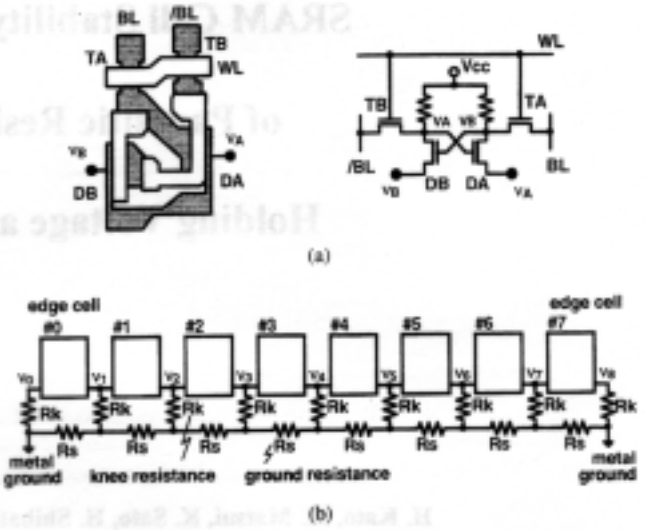

Fig. 1. The SRAM cell and its array structure. (a) The cell layout and its equivalent circuit. (b) The memory array structure. Each rectangular block corresponds to the single cell. The resistances R_k and R_s are the knee node resistance and the ground line resistance, respectively.

The data holding test is a method to confirm the SRAM reliability in manufacturing. At the beginning of the test, the SRAM is operated at a low supply voltage less than an ordinary operating voltage. After the recovery of the supply voltage to the ordinary operating voltage, the SRAM is involved in read operation. The cell behavior in the test sequence is mapped into a trajectory in a phase plane. An advantage of the data holding test is its flexibility to measure the cell at any location in a memory array. The validity of the trajectory analysis and the probing method is confirmed by the measurement on a 0.8-μm 1-Mb CMOS SRAM with poly-Si load cell.

II. Cell Stability and Data Holding Voltage

A. Configuration of Cell Array and Parasitic Resistances

In Fig. 1, the cell configuration in a memory array is illustrated. In (a), the layer diagram and its equivalent circuit are shown. The shaded and nonshaded areas represent the diffusion and first poly-Si layer, respectively. The poly-Si load cell is formed by the following components: two transfer

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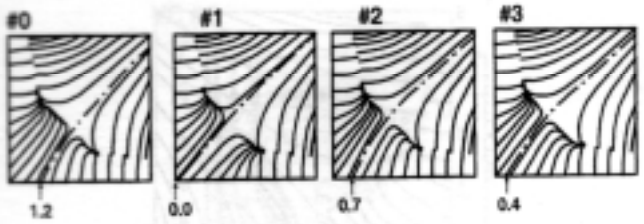

Fig. 7. The calculated trajectory diagrams for the half of the connected eight cells with the All-Low data.

after the terminal is not drawn for simplicity because the cell nodes are driven by subthreshold current and the trajectory has too many arrows. The minimum data hold voltage $V_{DH\,\min}$ is determined by the cross point of the divider line and the horizontal axis. This value depends on the cell number and the data pattern held by the memory array. The most unstable cell has the maximum $V_{DH\,\min}$ and it is the #0 cell (edge cell) when the memory array holds the All-Low data pattern. The #1 cell is the worst cell when the memory array maintains the All-High data pattern. In Fig. 7, the trajectory diagram for half of the unit memory array are shown when the holding data is All-Low. The another half cells have the mirror symmetry. Each diagram labeled by #0 to #3 corresponds to the cell labeled by the same number in Fig. 2(a). The data holding voltage is 1.2, 0.0, 0.7, and 0.4 V for the cell numbered by #0, #1, #2, and #3, respectively. The magnitude of $V_{DH\,\min}$ does not depend on the absolute value of the knee node voltages but it depends on the imbalance voltage of the two knee nodes of a cell.

We have also calculated the $V_{DH\,\min}$ for the array with the All-High data and the calculated values are summarized in Fig. 8 with the case for All-Low data. In this figure, the simulated data are represented by a solid line and the measured data are shown by the open circles with error bars. The simulated data confirm the $V_{DH\,\min}$ dependence on the cell number. The discrepancy between the simulated and measured data is caused by the parameter extraction and its variations in the memory array. The variations are caused by the fabrication distribution in the cell such as the layer misalignment and/or the circuit offsets such as in the local sense amplifier. The analysis including the variations will be important to maintain the device reliability in manufacturing system.

III. Scaling Trend of SRAM Cell

The scaling trend of the SRAM cell with respect to the parasitic resistances is summarized in Table I. There are parameters for three generations from 0.8-μm to 0.35-μm rules. The cell is poly-Si load type except for the 0.35-μm rule. For the 0.35-μm rule, the full-CMOS cell is used because of the immunity from defects [2]. The important quantity to analyze cell stability is the voltage of the edge cell, $V_{\rm edge}$, that is listed in the last row of the table. The voltage $V_{\rm edge}$ is determined by (1). The knee resistance R_k is constructed by the N^+ diffusion layer and the contact hole that connects the driver transistor source to the poly-Si ground line. The sheet resistance of the diffusion layer has the value 70 Ω/sq (where "sq" is the symbol of square) in the 0.8-μm rule device, and this value increases to 98 Ω/sq in 0.5-μm technology. This is because of the low temperature process introduced to restrict lateral impurity diffusion. In the

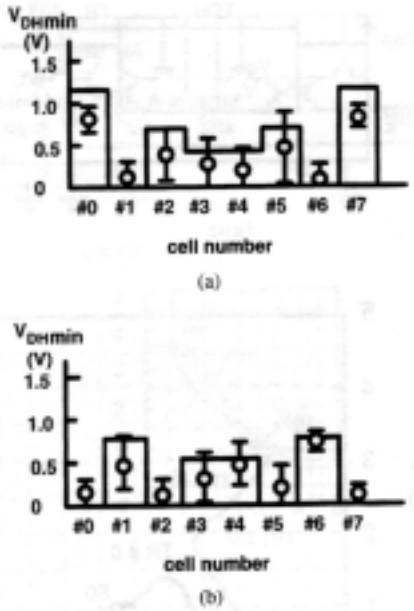

Fig. 8. The measured and the simulated data holding voltage $V_{DH\,\min}$ of a 0.8-μm SRAM. (a) The $V_{DH\,\min}$ dependence on the cell number with All-Low data pattern. (b) The $V_{DH\,\min}$ dependence with All-High data pattern.

0.35-μm rule, the value drastically decreases to 5 Ω/sq by the salicide technology. However, the contact resistance increases due to its diameter shrinkage, and the resistance R_k does not change drastically. The contact hole resistance will be a serious problem in the deep submicron device.

The ground line in the memory array is formed by direct contact layer (combined layer of N^+ diffusion and first poly layer) for the 0.8-μm technology and second poly-Si layer for the 0.5 and 0.35-μm technology. The sheet resistance of the second poly-Si layer increases in the 0.35-μm case compared with the 0.5-μm technology. In the 0.35-μm device, the thin second poly-Si layer thickness is required to maintain the fabrication flatness, and it affects the ground resistance R_s.

A large bridging span N_s is desired to increase the cell density. However, the increase of N_s enhances the resistance $R_{\rm eff}$ and affects the cell stability. The trade-off between the cell density and the cell stability is always a problem in any generation. The cell stability is also determined by the cell current $I_{\rm cell}$. The current $I_{\rm cell}$ is an important factor for the SRAM speed, and a large current is required for high-speed SRAM. The current of the 0.5-μm cell is depressed to a low level because the cell is developed for a medium-speed SRAM. However, the current of the 0.35 μm cell is high and the bridging span N_s has remained the same as for the 0.5-μm generation. In this generation, the cell density becomes low compared with the simple scaling trend because of the increase of contact frequency in the cell array. Anyway, the total effective resistance $R_{\rm eff}$ and the edge cell parasitic voltage $V_{\rm edge}$ increase from 0.5 to 0.35-μm rule devices.

IV. Summary

Cell stability is affected by an imbalance voltage between the knee nodes, and the voltage is determined by the knee

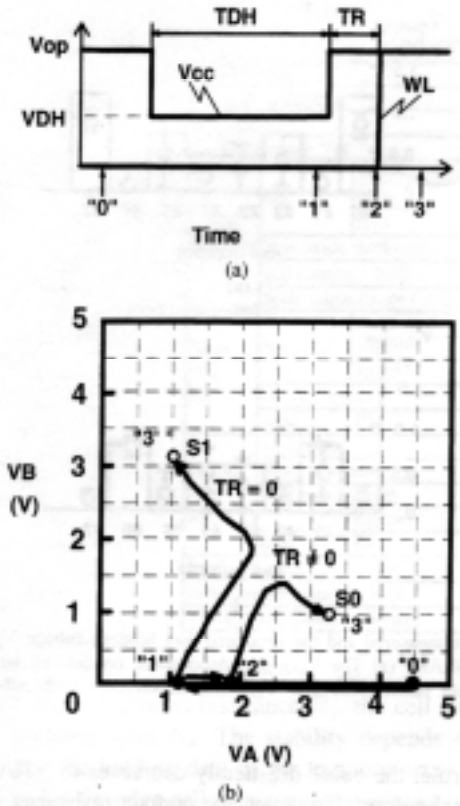

Fig. 5. The data hold test and the cell behavior in a phase diagram. (a) The test sequence for the supply voltage V_{cc} and the word line voltage WL. (b) The cell trajectory in a phase diagram composed by the storage nodes V_A and V_B.

We can detect the two SNM's by a test circuit with a probing wire from the cell storage nodes. However, the probing wire will affect the cell environment. To avoid this possibility and to measure the stability in an actual cell environment, we employ a method used in the data holding test.

C. Data Holding Test and Cell Trajectory Analysis

The data holding test is a method to evaluate the cell reliability by monitoring the minimum voltage to hold the cell data. This test can measure the cell stability in a practical environment in a memory array because it requires no probing wire. The test sequence and the cell behavior are illustrated in Fig. 5.

In the beginning of the test sequence, the supply voltage V_{cc} is set to the operating voltage V_{op} (= 4.5 V for the 0.8-μm SRAM) and the test data is written to the memory array at the time denoted by "0" in Fig. 5(a). Then the supply voltage is set to the holding voltage V_{DH} less than V_{op}. The SRAM is held at this voltage until the cell storage node in high level loses its charge and takes the level V_{DH}. The discharge process is visualized in the phase diagram in Fig. 5(b). This diagram is composed by two storage node voltages V_A and V_B. The point labeled by "0" corresponds to the state at the time indicated by "0" in Fig. 5(a). The discharge process is mapped to the line along the horizontal axis from "0"–"1". The charge at the storage node escapes to the supply node V_{cc} through the poly-Si load. The written data is not lost in this situation because the unaccessed cell has sufficient stability [1], [6].

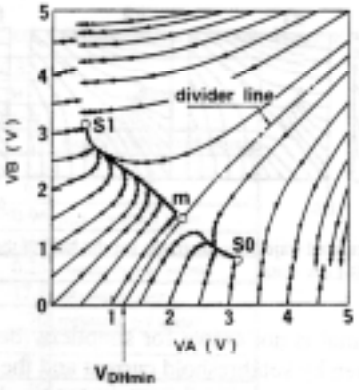

Fig. 6. The trajectory diagram of the edge cell with the All-Low data. Each trajectory from the axis corresponds to the cell behavior in read action.

The data upset occurs when the cell is involved in read cycle. In the cycle, the supply voltage V_{cc} is increased to the operating voltage V_{op} from the holding voltage V_{DH} to ensure the ordinary operation of the peripheral circuits (decoder, sense amplifier, and output buffers). This situation corresponds to the point denoted by "1" in Fig. 5(a) and (b). If a recovery time TR is allowed before the word line WL is opened, the discharged node recovers its voltage by the current from the poly-Si load. The load resistance is greater than $1T\,\Omega$, so that the charge up time is more than 10 ms [2]. For large recovery time, TR, the node voltage takes the trajectory from "1"–"2" in Fig. 5(b). When WL is turned on at the point "2" and the cell has gained enough stability, data upset does not occur. In Fig. 5(b), the cell trajectory from "2"–"3" represents a cell read with no data upset. If TR is negligible compared to the charge up time, there is possibility for the data upset. The path from "1" to "3'" in Fig. 5(b) corresponds to this data upset. In any way, the cell behavior after the WL is opened can be traced by the trajectory from the axes.

In Fig. 6, the behavior of the edge cell in a read action is summarized when the memory array has the All-Low data. The simulation is carried out with the 0.8-μm device parameters used in the Figs. 3 and 4. The capacitance parameter at the nodes V_A and V_B is 17.8 fF and is calculated from the geometric data of the poly-Si gate and diffusion layer of the driver and transfer transistors. The trajectory from the V_B axis corresponds to the cell behavior when the cell has Low data and the trajectory from the V_A axis is for the cell with High data. The trajectories from the sides opposite to the V_A and V_B axis are not used for the data hold analysis. However, they are useful to analyze the alpha-immunity [7], [8]. The arrows in each trajectory are placed every 50 ps time interval. We call this figure a trajectory diagram.

The one dashed line in Fig. 6 is called the divider line and it separates the curves into two regions. In the region right of the divider line, all trajectories reach a stable point S_0, and in the left region, the trajectories reach the other stable point S_1. The stable points S_0 and S_1 are the same points in Fig. 4(b). There are several trajectories which are terminated before reaching the stable points. The trajectory

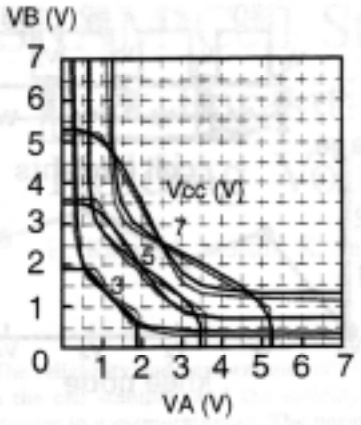

Fig. 3. The measured and the simulated superimposed characteristics of an isolated single cell fabricated by 0.8-μm rule process.

B. Static Noise Margin

The cell stability is visualized by superimposed characteristics of the cell inverters [5], [6]. In Fig. 3, the superimposed diagram of an isolated cell made by a 0.8-μm rule is shown. Here, the solid lines are the measured data and the dotted lines are simulated data. The axis denoted by V_A and V_B corresponds to the storage node voltage of the cell depicted in Fig. 1(a). The device parameters used for the simulation are extracted from the test element devices that share the same wafer with the 0.8 μm cell. The MOS drain current I_{D0} ($= I_{DS}$ at $V_{DS} = V_{GS} = 5$ V) is 0.23 mA for the transfer transistor and 0.85 mA for the driver transistor. The simulated and measured data are in good agreement except near the threshold voltage of the driver transistor. The discrepancy is caused by the model fitting around the threshold voltage. The two inverter characteristics are symmetric to the conversion of V_A and V_B axis. As described below, this symmetry is broken because of the parasitic resistances in an array.

The extracted parasitic resistance is 125 Ω for the knee node resistance R_k and 113 Ω for the ground resistance R_s. The cell current $I_{\rm cell}$ is 0.23 mA at 5 V supply voltage. The bridging span N_s is eight for the 0.8-μm memory array, so that the voltage $V_{\rm edge}$ is 0.17 V according to (1). In Fig. 4, the superimposed diagram for the edge cell is depicted when the memory array holds the All-Low data pattern. Fig. 4(a) is the schematic of the memory array used for the simulation. The symbol V_A is the input voltage of the A-inverter and its output is denoted by N_A. The notations V_B and N_B denote the same for the B-inverter. Fig. 4(b) is the result of the simulation. The output of A-inverter, N_A, is depicted for the axis of the B-inverter input, V_B, and vice versa for the B-inverter output. The inverter characteristic for A-inverter is deformed because of the parasitic voltage $V_{\rm edge}$. The solid line and dotted line correspond to the characteristic with and without the parasitic voltage $V_{\rm edge}$, respectively. The parasitic voltage at the knee node affects the threshold voltage and the resistance of the driver transistor because of the MOS back bias effect. This effect results in two kinds of deformation in the A-inverter characteristic. First, the curve shifts to the right because of the increase in the threshold voltage of the drain transistor.

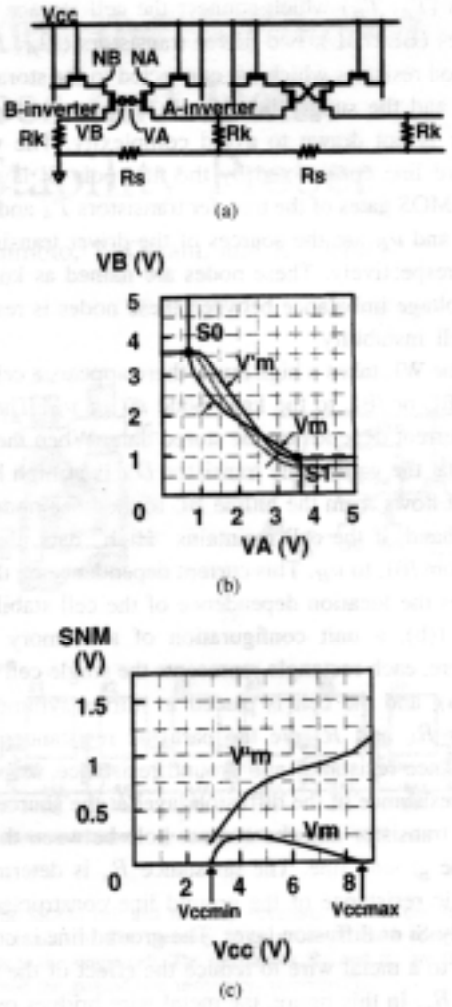

Fig. 4. The simulated inverter characteristics of the edge cell affected by the parasitic resistances. (a) The simulation circuit. (b) The superimposed inverter characteristics. The dotted line is for the isolated cell and the solid line for the correlated cell in a memory array. (c) The dependence of the static noise margin SNM on the supply voltage V_{cc}.

Second, the line slope decreases because of the increase in the drain transistor resistance. The points S_0 and S_1 correspond to the stable state of the cell during read action.

The SNM is the maximum width of the enclosed area of the superimposed characteristics as denoted in Fig. 4(b). When the diagram is symmetric, there is only one SNM. However, under the influence of the parasitic voltage, there are two values, $V_{\rm m}$ and $V'_{\rm m}$. The denotation $V_{\rm m}$ is used for the smaller SNM. In Fig. 4(c), the SNM dependence on the supply voltage V_{cc} is summarized. There is a range of V_{cc} for which $V_{\rm m} > 0$. The lower limit of the range corresponds to the minimum operating voltage $V_{cc\,\rm min}$ and the higher one is for the maximum operating voltage $V_{cc\,\rm max}$.

The existence of $V_{cc\,\rm max}$ is caused by the fact that the large cell current $I_{\rm cell}$ at high V_{cc} increases the voltage $V_{\rm edge}$. But, in practice, $V_{cc\,\rm max}$ is determined by the breakdown of the MOS transistor which is not included in this SPICE simulation. However, the mechanism pointed out in this paper suggests a possibility that the cell stability does not always increase while the voltage V_{cc} becomes large.

transistors (T_A, T_B) which connect the cell storage nodes to the bitlines (BL, /BL), two driver transistors (D_A, D_B), two poly-Si load resistors which are connected to the storage nodes (V_A, V_B) and the supply bus V_{cc}. In this figure, the poly-Si load layer is not drawn to avoid complexity. The wire WL is the word line constructed by the first poly-Si layer and it forms the MOS gates of the transfer transistors T_A and T_B. The nodes ν_A and ν_B are the sources of the driver transistors D_A and D_B, respectively. These nodes are named as knee nodes and the voltage imbalance between these nodes is responsible for the cell instability.

When the WL takes a high level, there appears a cell current from the BL or /BL to the knee node ν_A or ν_B. The path of this cell current depends on the stored data. When the cell has "Low" data, the gate of the transistor D_A is at high level and the current flows from the bitline BL to the knee node ν_A. On the other hand, if the cell maintains "High" data, the current appears from /BL to ν_B. This current dependence on the stored data causes the location dependence of the cell stability.

In Fig. 1(b), a unit configuration of a memory array is shown. Here, each rectangle represents the single cell depicted in Fig. 1(a), and the cell is placed in mirror symmetry. The resistances R_k and R_s are the parasitic resistances and are named as knee resistance and ground resistance, respectively. R_k is the resistance of the diffusion layer at the source node of the driver transistor and the contact hole between the source node to the ground line. The resistance R_s is determined by the parasitic resistance of the ground line constructed by the second poly-Si or diffusion layer. The ground line is connected frequently to a metal wire to reduce the effect of the parasitic resistance R_s. In this figure, the metal wire bridges over eight cells, and the connections are made beside the cells with the number #0 and #7. The cell density of a memory array is affected by this frequency of the connection, and the frequency is determined with the tradeoff between the cell density and the cell stability.

The parasitic resistances R_k and R_s affect the cell stability in read action. When a word line WL has a high potential level, current flows in the ground line from all cells controlled by the WL. The path of the cell currents depends on the data pattern written in the memory array. In Fig. 2, the current path and its effect on the knee node voltage are illustrated. The current path is indicated by an arrow from the knee node to the ground line. In Fig. 2(a), all cells have "Low" data (All-Low data) and, in Fig. 2(b), the cells maintain "High" data (All-High data). In the diagram, only half of the connected eight cells are shown because of the mirror symmetry of the data and the cell configuration.

The cell currents increase the knee node voltages and result in a voltage imbalance between two knee nodes in each cell. The stability of the cells are affected by each other because of the cell currents and the knee nodes voltages. The most unstable cell is the edge cell adjacent to the contact of the metal wire when the memory array has the All-Low data pattern. The voltage imbalance of the knee nodes of the edge cell, V_{edge},

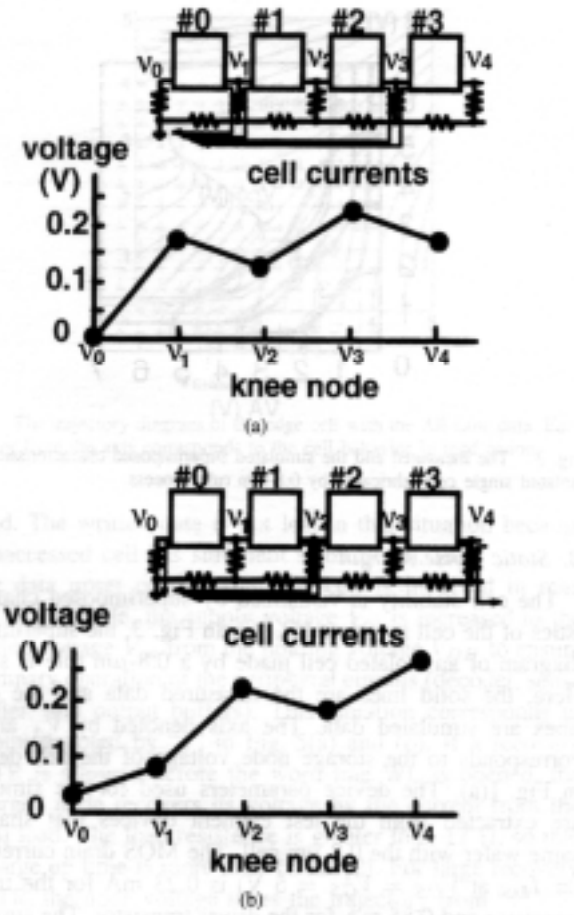

Fig. 2. The knee node voltage depends on the holding data and the cell location labeled by #0 to #3. Only half of the connected eight cells are illustrated because of the mirror symmetry. (a) The memory array holding the All-Low data. (b) The array with All-High data.

is represented as follows:

$$V_{\text{edge}} = I_{\text{cell}}\left(2R_k + \frac{N_s}{2}R_s\right). \tag{1}$$

Here, I_{cell} is the cell current per one cell in read action, and N_s is the bridging span of the metal ground line. The factor two, in front of R_k, is caused by the cell currents from the cells numbered by #0 and #1 to the knee node ν_1. The factor $N_s/2$ corresponds to the fact that the currents from half of the eight cells gather at the metal contact. We call the resistance in the right-hand side of (1) the effective resistance denoted by R_{eff} such that

$$R_{\text{eff}} = 2R_k + \frac{N_s}{2}R_s. \tag{2}$$

Migrating to a finer geometry process generally requires narrower wiring and longer bridging to increase the cell density, and both contribute to an increase in the effective resistance which affects the cell stability. Moreover, the low temperature process to restrict the lateral impurity diffusion and the increase of misalignment rate against the design rule enhances this tendency [1].

TABLE I
THE SCALING TREND OF THE CELL PARAMETERS. THE MAIN PARAMETER TO DETERMINE THE CELL STABILITY IS THE VOLTAGE V_{edge} IN THE LAST ROW

Designe rule			(μ m)	0.35	0.5	0.8	comment
Memory capacity			(b it)	16M	4M	1M	
Cell type				full-C	poly-Si	poly-Si	
Source voltage Vcc			(V)	3.3	5	5	standerd operation voltage
Cell charact.	size	width	(μ m)	1.7	3.5	5.6	
		hight	(μ m)	4.5	5.7	9.1	
		area	(μ m^2)	7.65	19.95	50.96	area = width x hight
	gate oxide thickness		(n m)	90	110	160	
	cell current Icell		(m A)	0.21	0.15	0.25	current in read action
	node capacitance Ccell		(f F)	4.5	8.1	17.8	data storage node
Knee resi. Rk	N+ diffu.	sheet resi.	(Ω /sq)	5	98	70	resistance per square
		width	(μ m)	0.74	1.4	1.4	
		length	(μ m)	0.36	2.51	2.3	
	contact resis.		(Ω)	100	20	10	contact resi. to poly-Si grand
	total Rk		(Ω)	102	196	125	Rk=sheet*length/width+cont.
Grand resi. Rs	wire layer			2poly	2poly	diff.+1poly	
	sheet resistance		(Ω /sq)	30	10	20	resistance per square
	wire size	width	(μ m)	1.02	4.5	0.9	
		length	(μ m)	1.7	3.7	5.1	equivalent to cell width
	total Rs		(Ω)	50	8	113	Rs=sheet*length/width
Bridging span Ns				16	16	8	grand line contacting span
Effective resistance Reff			(Ω)	604	456	702	Reff = 2Rk+Ns Rs/2
Voltage imbalance Vedge			(m V)	127	68	176	Vedge = Icell Reff

resistance R_k, the ground resistance R_s, the cell current I_{cell}, and the bridging span N_s. The stability depends on the cell location and the holding data of the memory array. The most unstable cell is the edge cell adjacent to the contact of the metal ground line when the array holds the All-Low data pattern. As geometry scaling proceeds, the effective resistance R_{eff} is influenced by many factors such as the shrinkage of the wiring width, low temperature processing, and the increase of the bridging span. The tradeoff between the cell stability and the cell density is a main concern in the design of the memory array. Moreover, for the high-speed SRAM, the increase of the cell current will be critical to realize the stable cell.

The dependence of the cell stability on the cell location has been probed by the data holding test, and the cell behavior in the test is analyzed by the trajectory diagram. The validity of the analysis is confirmed by the measurement of the 0.8-μm 1-Mb CMOS SRAM with poly-Si load cell. The data holding test provides a feasible probing method to measure the cell stability at any location under a practical cell environment in a memory array.

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